## **AMENDMENTS TO THE CLAIMS:**

1. (Currently amended) A semiconductor device, comprising:

a multi-layered insulation film formed on a semiconductor substrate, said multi-layered insulation film comprising:

a methyl silsequioxane (MSQ) layer;

a methylated hydrogen silsesquioxane (MHSQ) layer formed on and being in contact with said MSQ layer; and

an inorganic insulation layer formed on and being in contact with said MSHQ layer and comprising a member selected from the group consisting of silicon oxide, silicon nitride and silicon oxynitride, said inorganic insulation layer comprising an uppermost layer of said multi-layered insulation film, such that said MHSQ layer inhibits a peeling away of said inorganic insulation layer; and

a plurality of wires which are formed in grooves formed in said multi-layered insulation film, said MSQ layer, MHSQ layer and inorganic insulation layer of said multi-layered insulation film filling a space between said wires.

- 2. (Canceled)
- 3. (Canceled)
- 4. (Canceled)
- 5. (Currently amended) A semiconductor wafer, comprising:

a multi-layered insulation film formed on a surface of the wafer, said multi-layered insulation film comprising:

a methyl silsequioxane (MSQ) layer;

a methylated hydrogen silsesquioxane (MHSQ) layer formed on and being in contact with said MSQ layer; and

an inorganic insulation layer formed on and being in contact with said MHSQ layer and comprising a member selected from the group consisting of silicon oxide, silicon

nitride and silicon oxynitride, said inorganic insulation layer comprising an uppermost layer of said multi-layered insulation film, such that said MHSQ layer inhibits a peeling away of said inorganic insulation layer; and

a plurality of wires which are formed in grooves formed in said multi-layered insulation film, said MSQ layer, MHSQ layer and inorganic insulation layer of said multi-layered insulation film filling a space between said wires.

- 6. (Canceled)
- 7. (Canceled)
- 8. (Canceled)
- 9-30. (Canceled)
- 31. (Previously presented) The semiconductor device according to claim 1, wherein a dielectric constant of said MSQ layer is no greater than 3.5.
- 32. (Canceled)
- 33. (Canceled)
- 34. (Previously presented) The semiconductor device according to claim 1, wherein said MSQ layer comprises a thickness greater than a thickness of said MHSQ layer, and wherein said MSQ layer comprises a thickness greater than a thickness of said inorganic insulation layer.
- 35. (Canceled)
- 36. (Canceled)

- 37. (Previously presented) The semiconductor device according to claim 1, wherein a bottom of said grooves is formed on a same surface as said MSQ layer.
- 38. (Previously Presented) The semiconductor device according to claim 1, wherein said plurality of wires comprise copper wires.
- 39. (Canceled)
- 40. (Previously presented) The semiconductor device according to claim 42, wherein said MHSQ layer comprises a thickness of about 50 nm.
- 41. (Currently amended) A semiconductor device having a damascene wiring structure, said semiconductor device comprising:

a multi-layered insulation film formed on a semiconductor substrate, said multilayered insulation film having a plurality of recesses and comprising:

a methyl silsesquioxane (MSQ) layer;

a methylated hydrogen silsesquioxane (MHSQ) layer formed on and being in contact with said MSQ layer; and

an inorganic insulation layer formed on and being in contact with said MHSQ layer and comprising a member selected from the group consisting of silicon oxide, silicon nitride and silicon oxynitride, said inorganic insulation layer comprising an uppermost layer of said multi-layered insulation film, such that said MHSQ layer inhibits a peeling away of said inorganic insulation layer; and

an electroconductive film formed in a recess in said plurality of recesses, said MSQ layer, MHSQ layer and insulation layer of said multi-layered insulation film filling a space between recesses in said plurality of recesses.

42. (Currently amended) A semiconductor device comprising a multi-layered insulation film and a plurality of wires formed on a semiconductor substrate, said multi-layered insulation film comprising:

a methyl silsesquioxane (MSQ) layer;

a methylated hydrogen silsesquioxane (MHSQ) layer formed on and being in contact with said MSQ layer; and

an inorganic insulation layer comprising a member selected from the group consisting of silicon oxide, silicon nitride and silicon oxynitride, and formed on and being in contact with said MHSQ layer,

wherein said MSQ layer, MHSQ layer and insulation layer of said multi-layered insulation film fills a space between said wires in said plurality of wires, said inorganic insulation layer comprising an uppermost layer of said multi-layered insulation film, such that said MHSQ layer inhibits a peeling away of said inorganic insulation layer, and

wherein said plurality of wires are formed in grooves which are formed in said multilayered insulation film.

- 43. (Previously presented) The semiconductor device according to claim 1, wherein said MSQ layer, MHSQ layer and insulation layer of said multi-layered insulation film comprise uniform widths.
- 44. (Previously presented) The semiconductor device according to claim 1, wherein a surface of said insulation layer is substantially coplanar with a surface of said plurality of wires.
- 45. (Previously presented) The semiconductor device according to claim 1, wherein said MHSQ layer is formed by one of a plasma CVD and a spin coating process where said semiconductor substrate is continuously maintained in a plasma atmosphere.
- 46. (Previously presented) The semiconductor device according to claim 1, wherein said methylated hydrogen silsesquioxane (MHSQ) layer includes methylated hydrogen silsesquioxane (MHSQ) having repeating units shown by formulae I, II and III

$$\begin{bmatrix}
c_{H_3} \\
0 & \vdots \\
0
\end{bmatrix}$$

$$\begin{bmatrix}
0 & \vdots \\
0 & \vdots \\
0
\end{bmatrix}$$

$$\begin{bmatrix}
0 & \vdots \\
0 & \vdots \\
0
\end{bmatrix}$$
(III)

, and

wherein a molar ratio of II to a total of I, II and III is at least 0.2.

- 47. (Previously presented) The semiconductor device according to claim 1, wherein a thickness of a thickest portion of said MHSQ layer is less than a thickness of said MSQ layer.
- 48. (Canceled)
- 49. (Currently amended) A semiconductor device, comprising:

a multi-layered insulation film formed on a semiconductor substrate, said multi-layered insulation film comprising:

a methyl silsesquioxane (MSQ) layer;

a methylated hydrogen silsesquioxane (MHSQ) layer formed on and being in contact with said MSQ layer; and

an insulation layer formed on and being in contact with said MHSQ layer and comprising a member selected from the group consisting of silicon oxide, silicon nitride and silicon oxynitride, said insulation layer comprising an uppermost layer of said multi-layered insulation film, such that said MHSQ layer inhibits a peeling away of said insulation layer;

a plurality of gate electrodes formed on said semiconductor substrate; and

a plurality of impurity diffusion regions formed in the semiconductor substrate,

wherein said MSQ layer, MHSQ layer and insulation layer are formed on said plurality of gate electrodes, and

wherein a space formed between adjacent gate electrodes in said plurality of gate electrodes is filled with said MSQ layer.

50-52. (Canceled)

53. (Previously presented) The semiconductor device according to claim 1, further comprising:

a silicon nitride layer, said MSQ layer being formed on said silicon nitride layer and said grooves having a bottom defined by an upper surface of said silicon nitride layer.

54. (Canceled)

55-56. (Canceled)

57. (New) The semiconductor device according to claim 1, wherein a thickness of said plurality of wires in said grooves is in a range from 200nm to 500nm and said inorganic insulation layer comprises an upper surface which is coplanar with an upper surface of said plurality of wires, and

wherein said MHSQ layer inhibits a peeling away of said inorganic insulation layer during a planarization of said upper surface of said inorganic insulation layer and said upper surface of said plurality of wires.

- 58. (New) The semiconductor device according to claim 1, wherein said methyl silsequioxane (MSQ) layer has a thickness which is greater than a thickness of said methylated hydrogen silsesquioxane (MHSQ) layer and greater than a thickness of said inorganic insulation layer.
- 59. (New) The semiconductor device according to claim 46, wherein said molar ratio of II to a total of I, II and III is at least 0.5.